

## 4½ Digit Panel Meter Demonstrator/ Instrumentation Boards

Intersil's 8052A/7103A precision A/D converter pair with its multiplexed BCD outputs and digit drivers combines dual-slope conversion reliability with  $\pm 1$  count in 20,000 accuracy. The two chip system features performance characteristics such as 5pA input leakage, 0.002% linearity, auto-zero to  $10\mu V$  with drift less than  $1\mu V/^{\circ} C$ , and scale factor temperature coefficients of 3ppm/ $^{\circ} C$  (with external reference). With these outstanding features, the 8052A/7103A two chip system is ideally suited for LED display Digital Panel Meter (DPM) and Digital Multimeter (DMM) applications.

#### **DEMONSTRATOR BOARD**

Two versions of the complete circuit for a 4% digit DPM with  $\pm 2.0000$  volt full scale and LED readout will be discussed. The first version, the Demonstrator Board, is shown in schematic form in Figure 1. This circuit uses the internal reference of the 8052A for conversion reference and a buffered 2-inverter CMOS RC oscillator for the clock source. The Demonstrator Board contains all the components and displays for a 4% DPM on one, double-sided PC board. In addition, the BCD outputs, digit drivers, overrange, underrange, run/hold and busy lines from the 7103 are brought out to the edge connector making it possible to interface the DPM to a microprocessor or UART. The PC board layout diagram and component placement diagrams are shown in figures 2, 3 and 4.

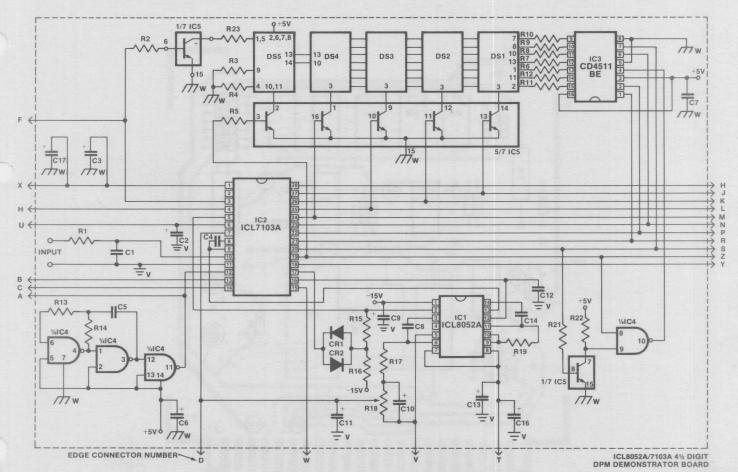
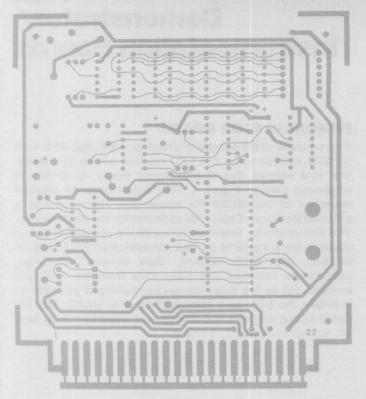


Figure 1: Demonstrator Board Schematic

## A019



FRONT
Figure 2: Demonstrator Board Component Side

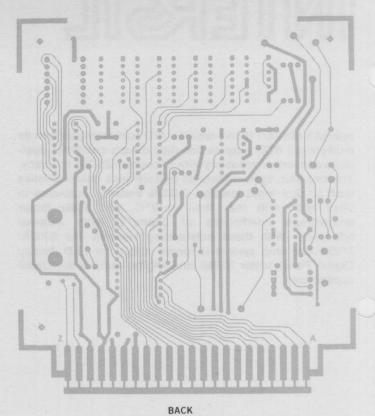


Figure 3: Demonstrator Board Back

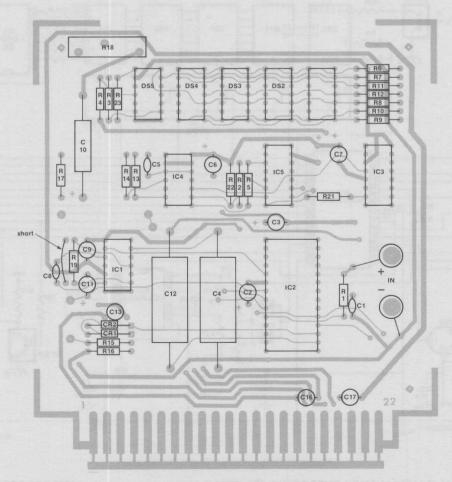


Figure 4: Demonstrator Board Component Placement

#### **INSTRUMENTATION BOARDS**

The schematic diagram in Figure 5 is for the 4½ Digit Instrumentation Boards which feature a lower component count, a separate front panel display board and a compact main board. The display board uses 5 similar LED Displays for the full digits and the polarity/½ digit, with the 7-segment decoder/driver on the reverse side of the board. The main board uses the 8052 reference, a CMOS clock circuit with variable frequency adjustment and has the BCD lines, digit driver lines, supply and ground lines, and input lines brought

out to the edge connector. Both boards use single-sided construction to simplify assembly and reduce fabrication costs. Figure 6 shows the main board PC layout with the component placement diagram in Figure 7. The display board artwork is shown in Figure 8 with component placement shown in Figures 9 and 10. Note that the displays are mounted on the trace side of the display board while the digit driver transistors, current-limiting resistors and the decoder/driver IC are mounted on the opposite side of the board.

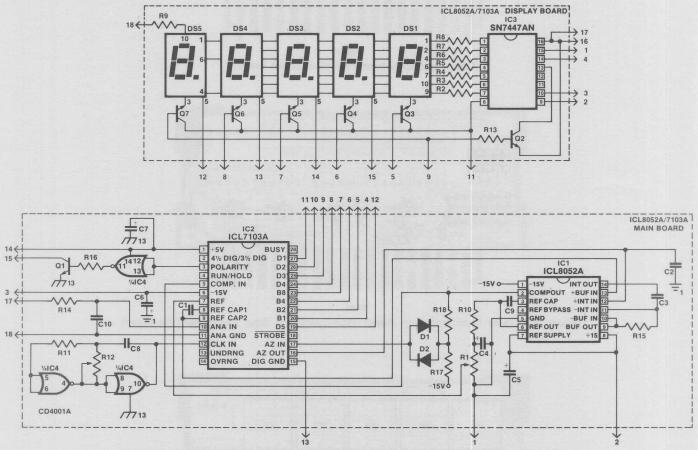


Figure 5: Instrumentation Board Schematic (Numerals refer to edge connector pin numbers)

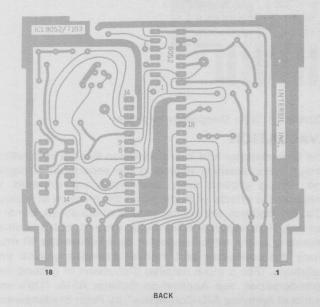


Figure 6: Main Instrumentation Board Back

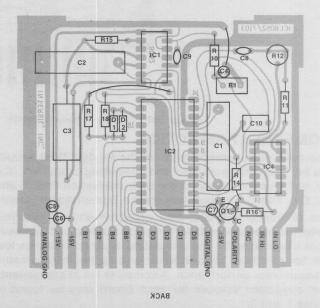


Figure 7: Main Instrumentation Board Component Placement

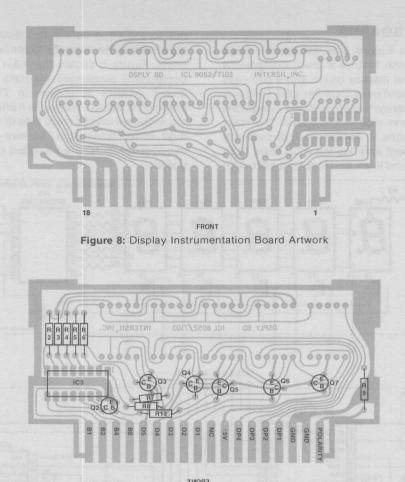


Figure 9: Display Instrumentation Board (Non-Conductor Side) Component Placement

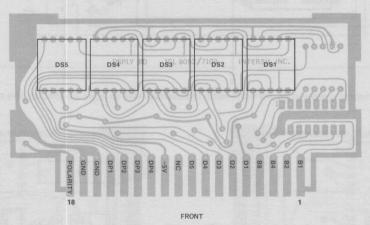


Figure 10: Display Instrumentation Board (Conductor Side) Component Placement

#### **COMPONENT SELECTION**

The only critical components for the  $4\frac{1}{2}$  digit DPM circuits are the reference, auto-zero and integrating capacitors, ( $C_1$ ,  $C_2$ , and  $C_3$  respectively for the Instrumentation Boards and  $C_4$ ,  $C_{12}$ , and  $C_{14}$  respectively for the Demonstrator Board). The reference and auto-zero capacitor should have low dielectric absorption (D.A.) for quick start-up and recovery from overload while the integrating capacitor requires low DA for minimum rollover error and optimum ratiometric measurement performance. A complete list of components and suggested sources for each board may be found in tables 1 and 2.

#### **EVALUATION**

The Demonstrator and Instrumentation Boards both reflect design considerations regarding the separation of digital and analog ground lines, and grounding priorities to minimize the effects of IR drops on the grounds of various IC's. For instance, the analog ground of the 8052A (pin 5) is not only kept separate from digital ground, but is in close proximity to the edge connector to minimize the IR drop along the conductor and, hence, minimize ground line variations. (For a more detailed discussion of ground line considerations, see Application Bulletin A018, "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood).

# Table I ICL8052A/7103A 4½ DIGIT DIGITAL PANEL METER

Electrical Parts List for Demonstrator Board

Reference Designation	Description	Recommended Manufacturer & Part Numbe
IC1	Analog A/D Converter	Intersil ICL8052A
IC2	Digital A/D Converter	Intersil ICL7103A
IC3	7-Segment Decoder/Driver	RCA CD4511BE
IC4	Quad CMOS Nand Gate, 2-Input	RCA CD4011AE
IC5	7-Transistor Array, Common Emitter	RCA CA3081
C1	0.1μF Ceramic Capacitor	Sprague 7CZ5U104X0050D1
C2,C3,C6,C7,C9- C11,C13,C16,C17	10μF Tantalum Capacitor	Kemet T39-C106-025AS
C4,C12	1.0μF Polypropylene Capacitor 20%, 200V dc	TRW X363UW
C5	100pF Mica Capacitor	Arco CM4FD101J03
C8	300pF Mica Capacitor	Arco CM4FD301J03
C14	0.22μF Polypropylene Capacitor	IMB GA2A224
R1,R19,R22	100KΩ ¼W Resistor	
R2,R14,R15,R21	39KΩ ¼W Resistor	
R3,R4	330Ω ¼W Resistor	
R5	2.2KΩ ¼W Resistor	
R6-R12,R23	120Ω ¼W Resistor	
R13	82KΩ ¼W Resistor	
R16	300KΩ ¼W Resistor	
R17	510Ω ¼W Resistor	
R18	1KΩ Trimmer	Beckman 76PR1K
CR1,CR2	Small Signal Diode	1N914
DS1-DS4	7-Segment LED Display	HP 5082-7653
DS5	±1 Polarity Display	HP 5082-7656

# Table II ICL8052A/7103A 4½ DIGIT DIGITAL PANEL METER Electrical Parts List for Instrumentation Board

Reference Designation	Description	Recommended Manufacturer & Part Number
IC1	Analog A/D Converter	Intersil ICL8052A
IC2	Digital A/D Converter	Intersil ICL7103A
IC3	7 Segment Decoder/Driver	Texas Instruments SN7447AN
IC4	Quad CMOS Nor Gate, 2 input	RCA CD4001AD
C1, C2	1.0 μF Polypropylene Capacitor	Plessey 171L105K160
C3	0.22 μF Polypropylene Capacitor	IMB GA2A224
C4 thru C7	10 μF Tantalum Capacitor	Kemet T39-C106-025AS
C8	100pF Mica Capacitor	Arco CM4FD101J03
C9	300pF Mica Capacitor	Arco CM4FD301J03
C10	0.1 μF Polyester Capacitor	Siemens B325600.1/10/100
R1	1kΩ Cermet Trimpot	Bourns 3299P
R2 thru R9	120Ω ¼W Resistor	
R10	510Ω ¼W Resistor	
R11	200k() ¼W Resistor	
R12	100k() Trimmer	Spectrol 62-3
R13	47k() 1/4W Resistor	
R14, R15	100K() ¼W Resistor	
R16	4.7K() 1/4W Resistor	
R17	300k() 1/4W Resistor	
R18	36k() 1/4W Resistor	
D1, D2	Small Signal Diodes	IN914
Q1 thru Q7	NPN Transistor	Motorola MPS 3704
DS1 thru DS5	7 Segment LED Display	Fairchild FND507

### A019

One problem that exists on both PC boards regarding supply line variations is that of the CMOS clock source. Since the supply for the RC oscillator is shared with the LED display, any variation in supply voltage due to the display reading will also vary the supply voltage to the oscillator. The point at which this variation becomes critical is when the display changes from a full scale reading to overrange; i.e., 19999 to 0000. When in overrange, the display alternates between a blank display (all segments off) and the 0000 overrange indication. The supply voltage to the CMOS oscillator varies enough to cause a shift in the clock frequency. This shift occurs during the signal integrate/reference integrate phase of conversion causing a low display reading just after overrange recovery. For instance, if the signal voltage is 1.99995 volts, the display reading should toggle between 1,9999 and overrange. However, the clock frequency shift causes the display to read 1.9992 just after the 0000 overrange display before returning to the 1.9999 reading. The severity of the reading variation after overrange recovery depends on the magnitude of the clock variation which gets back to the stability of the supply voltage line to the RC oscillator.

The clock supply voltage modulation has been minimized on both boards by separating the display supply lines from the clock supply line. To eliminate any clock frequency shift completely, a clock source using Intersil's LM311 voltage comparator in positive feedback mode (Figure 11) could be substituted.

Another problem encountered with the 8052A/7103A DPM is that of gross over-voltage applied to the input. Any voltage in excess of  $\pm 2.0000$  volts may cause the display to give an erroneous voltage indication. The reason this occurs is the integrator continues to ramp towards the supply (positive for negative input voltages, negative for positive inputs) until the

integrator output saturates. When this occurs, the integrator can no longer source (or sink) current required to hold the summing junction (Pin 11) at the voltage stored on the auto zero capacitor. As a result, the voltage across the integrator capacitor decreases sufficiently to give a false voltage reading.

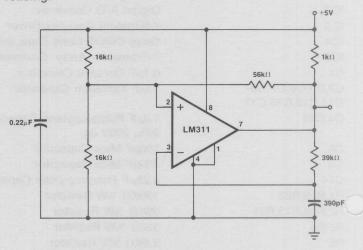


Figure 11: LM311 Clock Source

A simple solution to this problem is to use junction FET transistors across the integrator capacitor to source (or sink) current into the summing junction and prevent the integrator amplifier from saturating. Using an N channel and a P channel JFET, connect drains to pin 11 of the 8052A, sources to pin 14, the gate of the P channel to +15V, and the gate of the N channel to -15V (Figure 12). With the JFET's in this configuration, input voltages ranging from 2 to 6 volts positive and 2 to 10 volts negative will cause the correct overrange indication to occur.

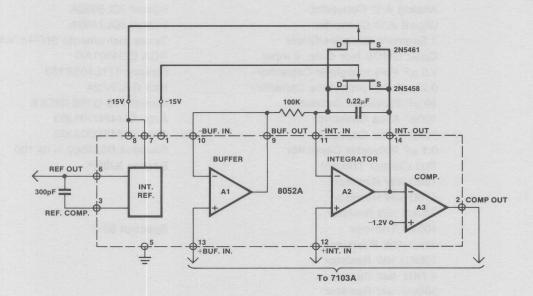
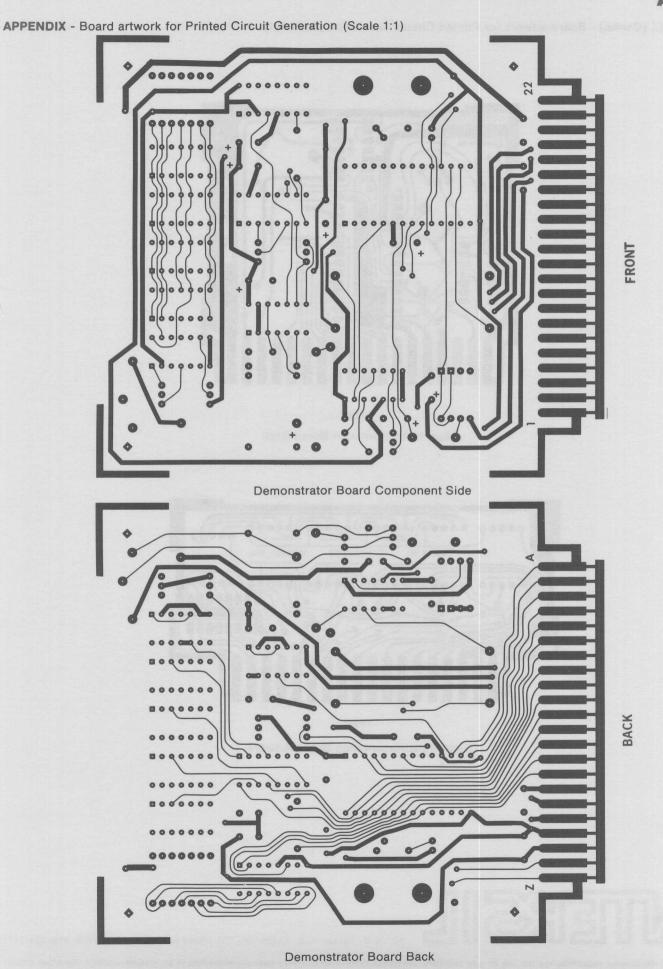
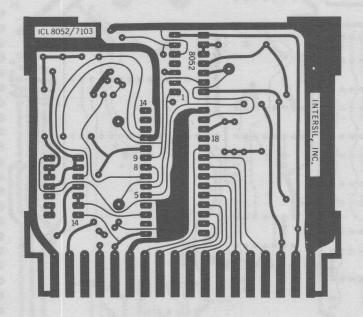


Figure 12: Gross Overvoltage Protection Circuit

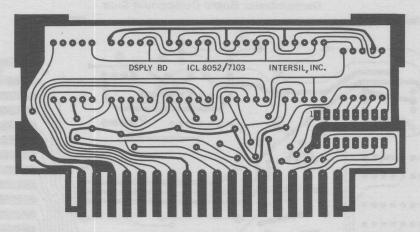


APPENDIX (Contd.) - Board artwork for Printed Circuit Generation (Scale 1:1)



BACK

Main Instrumentation Board Back



FRONT

Display Instrumentation Board Artwork



10710 N. Tantau Ave., Cupertino, CA 95014 (408) 996-5000 TWX: 910-338-0171

Intersil cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Intersil product. No other circuit patent licenses are implied. Intersil reserves the right to change the circuitry and specifications without notice at any time.

8 of 8